

# Gigabit Ethernet Core

GigE Vision® compliant IP Core for Altera Cyclone III and Stratix devices

GigE Vision® is a standardized communication protocol for vision applications based on the well known Ethernet technology. It allows easy interfacing between GigE Vision® devices and PCs running TCP/IP protocol.

Sensor to Image offers a set of IP cores and a development framework to build FPGA-based products with Gigabit Ethernet interface.

In principle there are two possibilities to realize systems with Gigabit Ethernet interfaces:

- use processor with Gigabit Ethernet interface
- use hardware - based solution

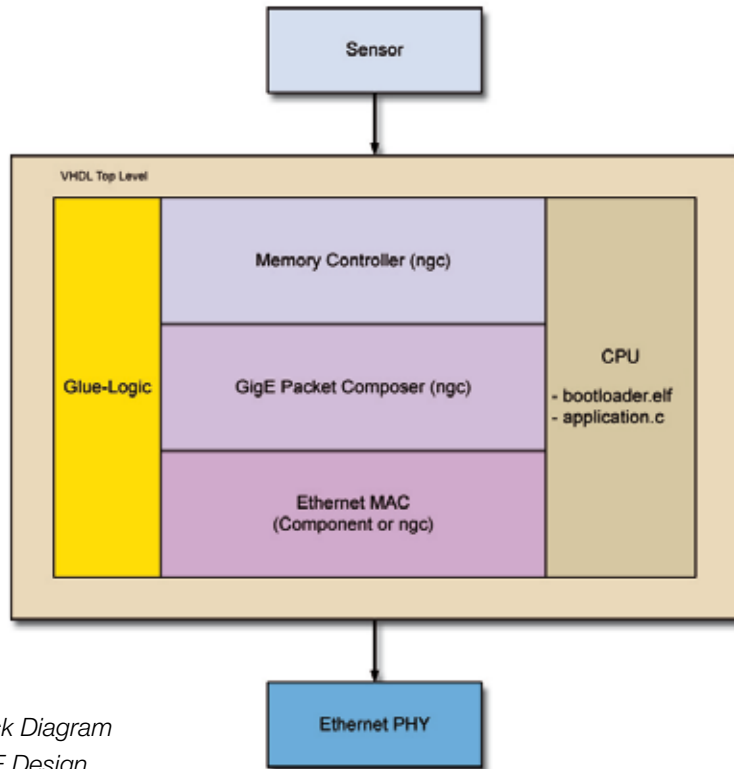
Sensor to Image developed a mixture of both concepts to combine advantages and avoid disadvantages of each approach.

This solution is made of a set of FPGA IP cores, which allows a maximum in performance at a small footprint and enough flexibility to realize custom solutions.

The following components are part of the design:

**Top Level Design**, which builds the interface between real hardware (e.g. sensor, external CPU, Ethernet Physical) and internal data processing. This module is delivered in source-code (VHDL), so it can be adapted and extended to custom hardware.

**Memory Controller** for different memory types, which allows frame buffering and image partitioning.



Block Diagram  
GigE Design

This is necessary to realize the packet resend function.

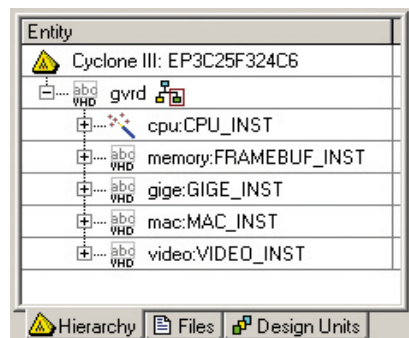
The **GigE Packet Composer** sends all data to the Ethernet MAC and realizes the high - speed "Streaming Channel" according to the GigE Vision® specification.

An **FPGA integrated CPU** (Nios® II processor) is for several non - time critical network and configuration tasks and it runs the "Control Channel". Software is written in C and can be extended by the customer. Some software parts are delivered as compiled files only (e.g. bootloader, GigE-controller), other parts are in source code.

The delivered design framework comes with all necessary design files and cores, Quartus® and EDS

project files and a Gigabit Ethernet camera and VGA-Out AddOn for the Altera® HSCMC - compliant FPGA boards, e.g. Cyclone® III FPGA Starter. This system should be used as reference design and evaluation board.

As a development environment, Altera Quartus II software and Nios EDS are used (not in scope of delivery).

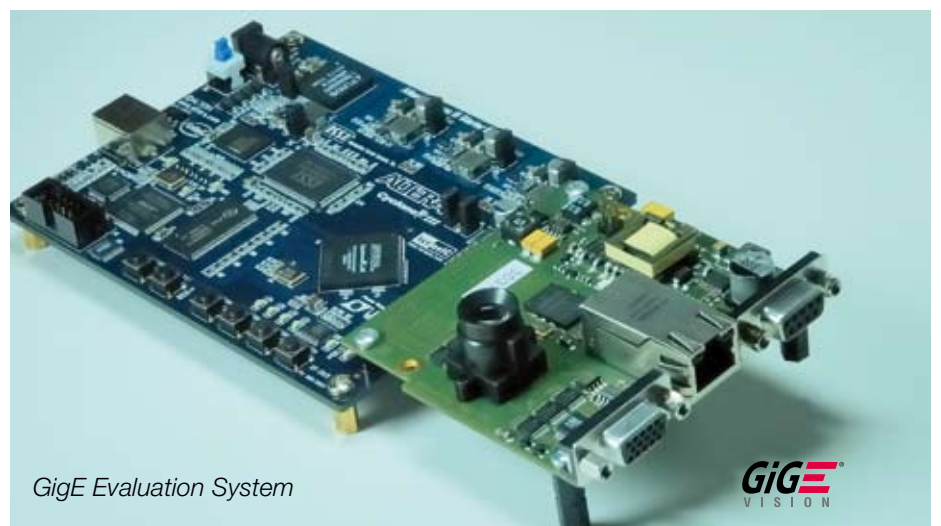


Quartus® Project Tree

AVAILABLE MODULES		CYCLONE® III	STRATIX® III/IV
MODULE	COMMENT		
Sync. bus as sensor interface incl. I <sup>2</sup> C/SPI core + C code	incl. 1 single tap sensor adaption	•	•
CameraLink incl. RS232 core + C code	base/medium incl. 1 single tap base camera adaption	•	•
GigE Core	project licence for CPU interface, packet composer, MAC interface, packet resend including SSRAM controller	•	•
Tri Mode MAC	Ethernet MAC core, only full-duplex supported	•	•
GigE Vision/GenICam software	Image Manager incl. filter driver, Transport Layer API, XML-File generation (Product and Service of Stemmer Imaging GmbH)		
Full sources, design, ...	on request		

other FPGA vendors on request

RESOURCES		CYCLONE® III	STRATIX® III	STRATIX® IV
MODULE				
GigE Packet Composer				
– Logic cells/ALMs		7800	4071	3806
– Registers		4464	4630	4558
– M9Ks		25	23	25
– DSPs		2	2	2
– PLLs		0	0	0
– Maximum clock frequency*		101 MHz	144 MHz	140 MHz
CPU system based on Nios II processor				
– Logic cells/ALMs		6167	3065	2924
– Registers		3726	3537	3473
– M9Ks		23	21	21
– DSPs		4	4	4
– PLLs		2	2	2
– Operating clock frequency		85 MHz	85 MHz	85 MHz
MAC				
– Logic cells/ALMs		969	483	433
– Registers		544	526	526
– M9Ks		0	0	0
– DSPs		0	0	0
– PLLs		0	0	0
– Maximum clock frequency		125 MHz	125 MHz	125 MHz
* 80 MHz required to reach maximum bandwidth of Gigabit Ethernet				



GigE Evaluation System

